

WoDiM 2006 Workshop Program

Santa Tecla Palace Hotel

Sunday June 25

18:00-21:00 REGISTRATION

Monday June 26

07:30 – 08:30 Registration

08:30 Welcome address

8:45 Session High-k I. Chair: Paul Hurley, Tyndall National Institute, Cork, Ireland

8:45 - Invited paper. Experimental and modeling study of NBTI in oxide and high k pFETs, Sufi Zafar, IBM, Yorktown

9:15 - Reliability aspects of Hf-based capacitors: breakdown and trapping effects, R. Duschl, M. Kerber, A. Avellan⁺, S. Jakschik⁺, U. Schroeder⁺, and S. Kudelka⁺ (Infineon Technologies AG, Munich, Germany; ⁺Infineon Technologies AG, Dresden, Germany)

09:30 - Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks, F. Crupi^(a), P. Srinivasan^(b,c), P. Magnone^(a), E. Simoen^(c), C. Pace^(a), D. Misra^(b), C. Claeys^(c,d) (^(a)DEIS, University of Calabria, Italy; ^(b)NJIT, Newark, USA; ^(c)IMEC, Belgium; ^(d)KU Leuven, Belgium)

9:45 - NBTI reliability of Ni FUSI/HfSiON gates: effect of silicide phase, A. Shickova, B. Kaczer, A. Veloso, M. Aoulaiche, M. Houssa, H. Maes, G. Groeseneken and J. A. Kitt¹, (IMEC, Belgium; ¹Assignee from Texas Instruments at IMEC, Belgium)

10 :00 - Characterisation of charge trapping in SiO₂/Al₂O₃ dielectric stacks by pulsed C-V, G. Puzzilli, B. Govoreanu*, F. Irrera, M. Rosmeulen*, J. Van Houdt* (University of Rome “La Sapienza”, Italy; *IMEC, Belgium)

10:15 - Negative Bias Stressing Interface Trapping Centers in Metal Gate Hafnium Oxide Field Effect Transistors Using Spin Dependent Recombination, C.J. Cochrane¹, P.M. Lenahan¹, J.P. Campbell¹, G. Bersuker², P. Lysaght², A. Neugroschel³ (¹The Pennsylvania State University, USA; ²SEMATECH, Austin, USA; ³University of Florida, USA)

10:30 – 11:00 Coffee break

11:00 Session High-k II. Chair: Chadwin Young, SEMATECH, Austin, USA

11:00 - Invited paper. Initial and PBTI-induced traps and charges in HfO₂/TiN stacks, Gilles Reimbold, CEA-LETI, Grenoble, France

11:30 - Reliability Screening of high-k Dielectrics based on Voltage Ramp Stress, A. Kerber¹, L. Pantisano², A. Veloso², G. Groeseneken², M. Kerber¹ (¹Infineon Technologies AG; ²IMEC, Infineon Technologies AG, Munich, Germany)

11:45 - Effective Work function Modulation control: the trick is in the dielectric !, L.Pantisano¹, V. V. Afanas²ev², T. Schram¹, S. Shamuilla², A Akheyar⁶, B.O'Sullivan^{1,3}, T. Conard¹, A. Stesmans², S. De Gendt^{1,3}, G. Groeseneken^{1,4}, P. Zimmerman⁵, M. M. Heyns¹ L.Ravel⁷ (¹IMEC, Belgium; ²Phys., ³Chem., and ⁴ESAT KUL, Belgium; ⁵Intel and ⁶Infineon assignees at IMEC ⁷Riber SA, France)

12:00 - Mechanism of O₂-anneal induced V_{th} shifts for Ru gated stacks, Z. Li^{a,b}, T. Schram^a, L. Pantisano^a, A. Stesmans^c, T.Conard^a, S. Shamuilia^c, V. V. Afanasiev^c, A. Akheyar^d, S. Van Elshocht^a, D. P. Brunco^e, W. Deweerdt^a, S. De Gendt^{a,f}, K. De Meyer^{a,b} (^aIMEC, Belgium; ^bESAT, ^cPhysics and ^fChemistry department, University of Leuven, Belgium; ^dInfineon and ^eIntel assignee at IMEC)

12:15 - Electron Spin Resonance Studies of Electrically Active Defects in the Near Si/Dielectric Interfacial Layer of Hafnium Oxide MOS Devices, J.T. Ryan¹, P.M. Lenahan¹, G. Bersuker², P. Lysaght², (¹The Pennsylvania State University, University Park, PA; ²SEMATECH, Austin, TX)

12:30 - Optimization of HfSiON using a Design of Experiment (DOE) approach on 0.45V Vt Ni-FUSI CMOS Transistors, A. Rothschild^a, R. Mitsuhashi^c, C. Kerner^a, X. Shi^a, J.L. Everaert^a, L. Date^b, T. Conard^a, O.Richard^a, C. Vrancken^a, R. Verbeeck^a, A. Veloso^a, A. Lauwers^a, M. De Potter^a, I. Debusschere^a, M. Jurczak^a, M. Niwa^c, P. Absil^a, S. Biesemans^a (^aIMEC, ^bApplied Materials, ^cMatsushita c/o IMEC, Leuven, Belgium)

12:45 - Distribution and generation of traps in SiO₂/Al₂O₃ gate stacks, I. Crupi^a, R. Degraeve^b, B. Govoreanu^b, D. P. Brunco^c, P. Roussel^b, and J. Van Houdt^b, (^aMATIS CNR-INFM, Catania, Italy; ^bIMEC, Leuven, Belgium; ^cIntel assignee at IMEC, Leuven, Belgium)

13:00 – 14:30 Lunch

14:30 Session NVMs I. Chair: Gabriella Ghidini, STMicroelectronics, Agrate, ITALY

14:30 - Invited paper. Phase Change Memory: a promising non volatile memory technology for the next decade, Roberto Bez, STMicroelectronics, Agrate, Italy

15:00 - Invited paper. Silicon Nanocrystals: Fundamental Physics & Memory Technology, R. Steimle, Freescale, Austin, USA

15:30 - Study of Nanocrystal Memory Integration in a 16 Mb Flash-like NOR Array, C. Gerardi¹, S.Lombardo², G.Costa¹, G.Ammendola¹, V. Ancarani¹, O. Brafa¹, D. Mello¹ (¹STMicroelectronics, Catania, Italy; ²CNR-IMM, Catania, Italy)

15:45 - High-K dielectrics for Inter-poly Application in Non Volatile Memories A. Sebastiani, R. Piagge, Modelli and G. Ghidini (STMicroelectronics, Central R&D, Agrate Brianza, Italy)

16:00 - Ionising Radiation and Electrical Stress on Nanocrystal Memory Cell Array A. Cester¹, A. Gasperin¹, N. Wrachien¹, A. Paccagnella¹, V. Ancarani², and C. Gerardi² (¹Dipartimento di Ingegneria dell'Informazione, Università di Padova, Italy; ²ST Microelectronics, Catania, Italy)

16:15 - Self-limited oxidation of Si nanocrystals generated by ultra-low-energy ion-beam-synthesis in SiO₂ thin films, C. Bonafos¹, S. Schamm¹, H. Coffin¹, N. Cherkashin¹, G. Ben Assayag¹, A. Claverie¹, P. Dimitrakis², P. Normand², V. Paillard³, M. Carrada³ (¹CEMES-CNRS, Toulouse, France; ²Institute of Microelectronics, NCSR 'Demokritos', Aghia Praskevi, Greece; ³LPST, Université Paul Sabatier, Toulouse, France)

16:30 - Pulsed Tunnel Operating Non Volatile Flash Memories With SILC Reduction, F. Irrera, A. Chimenton*, P. Olivo* (University of Rome "La Sapienza", Electronics Department, Italy; *University of Ferrara, Dipartimento di Ingegneria, Italy)

16:45 - HfSiO/SiO₂- and SiO₂/HfSiO/SiO₂-Gate Stacks for Non-Volatile Memories T. Erlbacher¹, M.P.M. Jank¹, M. Lemberger¹, A.J. Bauer², H. Ryssel^{1,2} (¹University of Erlangen-Nuremberg, Germany; ²Fraunhofer Institute of Integrated Systems and Device Technology, Erlangen, Germany)

17:30- 20:00 Poster session

Tuesday June 27

8:30 Session Ultra-thin oxynitrides. Chair: Sufi Zafar, IBM, Yorktown Heights, USA

08:30 - Invited paper. Channel hot carrier effects in nMOSFET devices of advanced submicron CMOS technologies, Giuseppe La Rosa, IBM Microelectronics, Hopewell Junction, NY, USA

09:00 - Invited paper. Gate oxide breakdown in FET devices and circuits: From nanoscale physics to system-level reliability, Ben Kaczer, IMEC, Leuven, Belgium

09:30 - Impact of Strained-Channel n-MOSFETs with a SiGe virtual substrate on dielectric interface quality evaluated by low frequency noise measurements, G. Neau^{2,1}, F. Martinez¹, M. Valenza¹, J.C. Vildeuil², E. Vincent², F. Boeuf², F. Payet², K. Rochereau³, (¹IES-CEM2-UNIVERSITE MONTPELLIER II-UMR CNRS, France; ²ST Microelectronics, Crolles, France; ³Philips Semiconductors, Crolles, France)

09:45 - Random Telegraph Signal noise: a sensitive and nondestructive tool for gate oxide single trap characterization, C. Leyris^{2,1}, F. Martinez¹, M. Valenza¹, A. Hoffmann¹, J-C. Vildeuil², (¹Centre d'Electronique et de Micro-optoélectronique de Montpellier, France; ²ST Microelectronics, Crolles, France)

10:00 - Thermal oxidation of MBE SiGe films: Ge segregation and defects injection, A. Terrasi^a, A. Grasso^a, C. Bongiorno^b, S. Mirabella^c, L. Romano^a, M.G. Grimaldi^a, (^aCNR-INFM MATIS, Catania & Dipartimento di Fisica e Astronomia, Università di Catania, Italy ; ^bCNR-IMM Catania, Italy ; ^cCNR-INFM MATIS, Catania, Italy)

10:15 - Low-Frequency noise in hot-carrier degraded MOSFETs, C. Salm, E. Hoekstra, J. Kolhatkar, A. Hof, H. Wallinga, J. Schmitz, (MESA+ Institute for nanotechnology, University of Twente, Semiconductor Components Group, AE Enschede, The Netherlands)

10:30 – 11:00 Coffee break

11:00 Session High-k III. Chair: Hans-Joachim Muessig, IHP, Frankfurt (Oder), Germany

11:00 - Invited paper. Non-Si Nanotechnologies for low power high performance logic applications, Paul Zimmerman, Intel Corporation, Santa Clara, USA

11:30 - Electrical Characterization of Crystalline Gd₂O₃ Gate Dielectric MOSFETs Fabricated by Damascene Metal Gate Technology, R. Endres, Y. Stefanov and U. Schwalke (Institute for Semiconductor Technology and Nanoelectronics, Darmstadt University of Technology, Germany)

11:45 - “High-k” interfacial layer for scaled HfO₂ gate stacks, C. Marchiori¹, B. Mereu¹, M. Sousa¹, A. Guiller¹, H. Siegwart¹, J.-P. Locquet¹, C. Rossel¹, R. Germann¹, J. Fompeyrine¹, J. W. Seo², C. Dieker², (¹IBM Research GmbH, Zurich Laboratory, Rueschlikon, Switzerland; ²IPMC-EPFL, Lausanne, Switzerland and Advanced Materials & Metrology, MosBeam Foundation, Lausanne, Switzerland)

12:00 - Effects of post-annealing treatment on rare earth high-k dielectrics on germanium, S.F. Galata¹, E.K. Evangelou², Y. Panagiotatos¹, A. Sotiropoulos¹, and A. Dimoulas¹, (¹MBE laboratory, Institute of Materials Science, NCSR DEMOKRITOS, Athens, Greece; ²Physics Department, University of Ioannina, Greece)

12:15 - Impact of Al-, Ni-, TiN-, and Mo metal gates on MOCVD-grown HfO₂ and ZrO₂ high-k dielectrics, Abermann S.¹, Efavi J.², Sjoblom G.³, Lemme M.², Olsson J.³, and Bertagnolli E.¹, (¹Institute of Solid State Electronics, Vienna University of Technology, Austria; ²Microelectronic Center, Aachen, Germany; ³Solid State Electronics Division, Uppsala University, Sweden)

12:30 - Epitaxial growth of LaAlO₃ on silicon using interface engineering, C. Merckling^{1,2}, G. Delhaye¹, M. El-Kazzi¹, S. Gaillard², Y. Rozier³, L. Rapenne⁴, B. Chenevier⁴, O. Marty⁵, G. Grenet¹, M. Gendry¹, Y. Robach¹, G. Hollinger¹, (¹LEOM-Ecole Centrale de Lyon, Ecully, France; ²ST Microelectronics, Crolles, France; ³LPM-INSA de Lyon, Villeurbanne, France; ⁴LMGP, Saint Martin d'Hères, France; ⁵LENaC, Villeurbanne, France)

12:45 - Growth and interface engineering of SrTiO₃ films on silicon by injection MOCVD, O. Salicio¹, L. Auvray¹, S. Lhostis¹, I. Matko¹, L. Hubert-Pfalzgraf², B. Hollander³, T. Schroeder⁴, F. Ducroquet⁵, N. Rochat⁶, C. Dubourdieu¹, (¹Laboratoire des Matériaux et du Génie Physique, UMR CNRS, France; ²Institut de Recherche sur la Catalyse, UPR CNRS, France; ³Institut für Schichten und Grenzflächen, Jülich, Germany; ⁴IHP-Microelectronics, Frankfurt (Oder), Germany; ⁵Institut de Microélectronique, Electromagnétisme et de Photonique, Grenoble, France; ⁶CEA Grenoble, DRT/DTS-LETI/SCPC, Grenoble, France)

13:00 – 14 :30

Lunch

PARALLEL SESSIONS

Sala Congressi

14:30 Session Measurements. Chair: Gérard Sarrabayrouse, LAAS-CNRS, Toulouse, France

14:30. Invited paper. Electrical Characterization Techniques for the High-k Era. Chadwin D. Young, Dawei Heh, Arnost Neugroschel*, Rino Choi, Chang Yong Kang, and Gennadi Bersuker (SEMATECH, Austin, U.S.A; *permanently at the Univ. of Florida, Gainesville).

15:00. Accurate Determination of Flat Band Voltage in advanced MOS structure

Charles Leroux¹, Gérard Ghibaudo² and Gilles Reimbold¹ (¹CEA-LETI, Grenoble Cedex 9, France; ²IMEP, Grenoble Cedex, France).

15:15. Worn-out oxide MOSFET characteristics: Role of gate current and device parameters on a current mirror. J.Martín-Martínez¹, R.Rodríguez¹, M.Nafría¹, X.Aymerich¹ and J.H.Stathis² (¹Dept. d'Enginyeria Electrònica.Universitat Autònoma de Barcelona, Bellaterra, Spain; ²IBM SRDC, Yorktown Heights, NY USA).

15:30. Application of an MOS tunnel transistor for measurements of the tunneling parameters and of the parameters of electron energy relaxation in silicon. I.Grekhov¹, G.G.Kareva², S.E.Tyaginov¹, M.I.Vexler¹ (¹ Ioffe Physico-Technical Institute, St Petersburg, Russia; ² St Petersburg State University, Institute for Physics, St Petersburg, Russia).

15:45. Quantitative Oxide Charge Determination by Photocurrent Analysis. M. Rommel¹, A.J. Bauer¹, and H. Ryssel^{1, 2} (¹ Fraunhofer Institute of Integrated Systems and Device Technology, Erlangen, Germany; ² Chair of Electron Devices, University of Erlangen, Germany).

16:00. Extracting the relative dielectric constant for “high – k layers” from CV measurements - errors and error propagation. O. Buiul, S. Hall¹, O. Engstrom², B. Ræiissi², M. Lemme³, P. K. Hurley⁴, K. Cherkaoui⁴ (¹ University of Liverpool, Liverpool, UK; ²Chalmers University of Technology, Sweden; ³AMO GmbH, Aachen, Germany; ⁴ Tyndall National Institute, University College Cork, Cork. Ireland).

16:15. Test Structures for Dielectric Spectroscopy of Thin Film at Microwave Frequencies. Nicola Del monte¹, Bernard Enrico Watts² (¹ Dipartimento di Ingegneria dell'Informazione, University of Parma, Parma, ITALY; ² Istituto IMEM/CNR, Parma, ITALY).

16:30-17:00 Coffe break

Sala Congressi

17:00 Session Theory and modelling. Chair: Cosimo Gerardi, STMicroelectronics, Catania

17:00. Invited paper. Density functional theory of high-k dielectric gate stacks. Alex Demkov (Department of Physics, The University of Texas at Austin, Austin, Texas, USA).

17:30. Dielectric properties of complex crystalline and amorphous high-k oxides. P. Delugas^{1,2}, V. Fiorentini^{1,2}, A. Filippetti¹, and G. Pourtois³ (¹SLACS-CNR and University of Cagliari, Italy; ²Philips Research, Leuven, Belgium; ³IMEC, Leuven, Belgium).

17:45. Full-band tunneling in high-κ dielectric MOS structures. F. Sacconi¹, J.M.Jancu², M. Povolotskyi¹, A. Di Carlo¹ (¹Dept. Electronic. Eng., University of Rome "Tor Vergata", Rome, Italy; ²Laboratoire de photonique et de Nanostructures, CNRS, Marcoussis, France).

18:00. Negative Bias Temperature Instability Modeling for High-Voltage Oxides at Different Stress Temperatures. R. Entner¹, T. Grasser¹, H. Enichlmair², and R. Minixhofer² (¹Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics, TU Wien, Wien, Austria; ²Austriamicrosystems, Unterpremstaetten, Austria).

18:15. Electronic structure of defects in dielectrics with and without electronic correlation. Vincenzo Fiorentini, Alessio Filippetti, and Giorgia M. Lopez (SLACS/CNR-INFN and University of Cagliari, Italy).

18:30. High-K dielectric deposition in 3D architectures: the case of Ta2O5 deposited with organometallicprecursor TBTDET. L. Pinzelli^{1,2}, M. Gros-Jean¹, Y. Bréchet², F. Volpi² (¹STMicroelectronics, Crolles, France; ²Institut National Polytechnique of Grenoble, LTPCM-UMR CNRS, Saint Martin d'Hères, France).

18:45. VSP – A Gate Stack Analyzer. M. Karner¹, A. Gehring², M. Wagner¹, R. Entner¹, S. Holzer¹, W. Goes¹, M. Vasicek¹, T. Grasser¹, H. Kosina¹, and S. Selberherr¹ (¹Institute for Microelectronics, TU Wien, Wien, Austria; ²AMD Saxony, Dresden, Germany).

19:00 - Templates for LaAlO3 epitaxy on silicon, Pierre Boulenc^{***}, Isabelle Devos^{*}, (*Institut d'Electronique de Microélectronique et de Nanotechnologie, Département ISEN, Lille, France; ^{***}STMicroelectronics, Crolles, France)

Sala dei Re

14:30 Session Novel materials, substrates. Chair: Montserrat Nafria Maqueda, Universitat Autònoma de Barcelona, Spain

14:30. Invited paper. Silicon Nanostructures in Dielectrics for Microphotonics. Francesco Priolo (MATIS CNR-INFM and Dipartimento di Fisica e Astronomia, Univ. di Catania, Catania, Italy).

15:00. The influence of hydrogen and nitrogen on the formation of Si nanoclusters embedded in sub-stoichiometric silicon oxide layers. Liliana Caristia¹, Corrado Spinella², Giuseppe Nicotra², Corrado Bongiorno², Nicola Costa¹, Sebastiano Ravesi¹, Salvo Coffa¹ (¹STMICROELECTRONICS, Catania, Italy; ²Istituto per la Microelettronica e Microsistemi – CNR, Catania, Italy).

15:15. RTA effects on the formation process of embedded luminescent Si nanocrystals in SiO₂. T. S. Iwayama¹, T. Hama² and D. E. Hole³ (¹Department of Physics, Aichi University of Education, Japan; ²Department of Information and Systems Engineering, Kanazawa University, Japan; ³Department of Engineering and Design, University of Sussex, United Kingdom).

15:30. Silicon dioxide modifications for biosensing applications. Sebania Libertino, Manuela Fichera and Salvatore Lombardo (CNR – IMM sez. Catania, Catania, Italy).

15:45. High Quality Gate Insulator Film Formation on SiC using by Microwave-Excited High-Density Plasma. Koutarou Tanaka, Hiroaki Tanaka, Akinobu Teramoto¹, Shigetoshi Sugawa, and Tadahihiro Ohmi¹ (Tohoku University, Aoba-ku Sendai, Japan; ¹New Industry Creation Hatchery Center, Tohoku University, Aoba-ku Sendai, Japan).

16:00. Optical characterization of Si-rich Silicon Nitride films prepared by Low Pressure Chemical Vapor Deposition. V. Em. Vamvakas, N. Vourdas and S. Gardelis (Institute of Microelectronics, NCSR “Demokritos”, Aghia Paraskevi, Athens, Greece).

16:15. Electrical characterization of gold nanocrystals in SiO₂ films: a proposal for a prototype of an integrated Single Electron Transistor-MOS device at room temperature. F. Ruffino¹, M. G. Grimaldi¹, F. Giannazzo², F. Roccaforte², V. Raineri² (¹INFM-MATIS and Dipartimento di Fisica e Astronomia, Università di Catania, Catania, Italy; ²CNR – IMM, Catania, Italy).

16:30 – 17:00 Coffe break

Sala dei Re

17:00 Session BEOL, MEMS. Chair: Ben Kaczer, IMEC, Leuven, Belgium

17:00. Dielectric thin films for MEMS-based optical sensors. M. Martyniuk, J. Antoszewski, C.A. Musca, J.M. Dell, and L. Faraone (The University of Western Australia, Crawley, WA, Australia)

17:15. Passivation issues in Active Pixel CMOS Image Sensors. J. L. Regolini, D. Benoit and P. Morin (STMICROELECTRONICS, Crolles, FRANCE).

17:30. Non-linearity of High-k MIM Capacitors. Ch. Wenger¹, Th. Schröder¹, J. Dabrowski¹, R. Sorge¹, H.-J. Müssig¹, S. Pasko² and Ch. Lohe² (¹IHP Microelectronics, Frankfurt Oder, Germany; ²AIXTRON AG, Aachen, Germany).

17:45. Refined electrical analysis of two charge states transition characteristic of “borderless” silicon nitride. G. Beylier^{1,2}, S. Bruyère¹, D. Benoit¹, G. Ghibaudo² (¹STMICROELECTRONICS, Crolles, France; ²IMEP, ENSERG, Grenoble Cedex 1, France).

18:00. Modification of porous ultra low-k dielectric by electron beam irradiation. C. Guedj¹, G. Imbert², E. Martinez¹, C. Licitra¹, N. Rochat¹, V. Arnal², M. Aimadeddine², A. Toffoli¹, L. Arnaud¹, V. Girault² (¹CEA-Leti, Grenoble Cedex, France; ²STMICROELECTRONICS, Crolles cedex, France).

18:15. Kinetics of conduction-related voltage instabilities in thick nitride/oxide dielectrics. S.B. Evseev (Philips Semiconductors, Gerstweg 2, Nijmegen, The Netherlands).

18:30. Characterizations of high resistivity TiN_xO_y thin films for application in thin film resistors. Nguyen Duy Cuong¹, Dong-Jin Kim², Byoung-Don Kang^{1,2}, Chang Soo Kim³, and Soon-Gil Yoon¹ (¹Chungnam National University, Daejeon, Korea; ²KMC technology, Panam Techno-Town 103, Panam-dong 239-2, Dong-gu, Daejeon, Korea; ³Korea Research Institute of Standards and Science, Daejeon, Korea).

18:45. Development of embedded capacitor with bismuth-based pyrochlore thin films deposited on polymer substrates at room temperature for printed circuit board applications. Jong-Hyun Park¹, Soon-Gil Yoon¹, Jeong-Won Lee², Hyung-Dong Kang², Yeoul-Kyo Chung², and Yong-Soo Oh² (¹Chungnam National University, Daejeon, Korea; ²Samsung Electro-Mechanics Co. LTD, Maetan3-Dong, Yeongtong-Gu, Suwon, Gyunggi-Do, Korea).

20:30 WORKSHOP BANQUET

Wednesday June 28

8:30 Session High-k IV. Chair: Felice Crupi, Università Calabria, Rende, ITALY

08:30 - MOCVD of TaN Films for Metal Gate Application using Novel Single-Source Precursors and TBTDET, M. Lemberger¹, A. Baunemann², A.J. Bauer³, H. Ryssel^{1,3}, (¹University Erlangen-Nuremberg, Germany; ²Ruhr-University Bochum, Germany; ³Fraunhofer Institute of Integrated Systems and Device Technology, Erlangen, Germany)

08:45- Studying the CMOS process compatibility of Pr-silicate layers on Si(001): Physical, electrical, thermal and etching properties, T. Schroeder, G. Lupina, Ch. Wenger, J. Dabrowski, H.-J. Müssig, (IHP Microelectronics, Frankfurt Oder, Germany)

09:00 -Defects induced anomalous breakdown kinetics in Pr2O3 by micro and nano characterization, P. Fiorenza^{# §}, R. Lo Nigro[#], S. Lombardo[#], V. Raineri[#], R. G. Toro[§], G. Malandrino[§] and I. L. Fragalà[§], ([#]CNR-IMM, Catania, Italy; [§]Dipartimento di Scienze Chimiche, Università di Catania, Italy)

09:15 - Electrical and structural properties of ALD hafnium silicate thin films, I.Z. Mitrovic, O. Buiu, S. Hall, C. Bungey*, T. Wagner**, W. Davey, Y. Lu, (University of Liverpool, Department of Electrical Eng. and Electronics, United Kingdom; *J. A. Woollam Co Inc., Lincoln, Nebraska, USA; **LOT Oriel, Dortmund, Germany)

09:30 - Effective Work function of Ni-Silicide/HfO₂ Gate Stacks Measured with X-ray Photoelectron Spectroscopy, Yu. Lebedinskii and A. Zenkevich, (Moscow Engineering Physics Institute, Russian Federation)

9:45 - Experimental observation of temperature-dependent Flat Band Voltage transients on high-k Dielectrics, S. Dueñas, H.Castán, H.García, L.Bailón, J.Gómez, K. Kukli^{1,2}, M.Ritala² and M. Leskelä², (Universidad de Valladolid, Spain; ¹University of Tartu, Estonia ; ²University of Helsinki, Finland)

10:00 - Degradation kinetics of ultrathin HfO₂ layers on Si(100) during vacuum annealing monitored with in situ XPS/LEIS and ex situ XTEMAFM, Yu. Lebedinskii¹, A. Zenkevich¹, G. Scarel², M. Fanciulli², A. Baturin³, N. Lubovin³, (¹Moscow Engineering Physics Institute, Russia; ²National Laboratory MDM-CNR, Italy; ³Moscow Technical Physics Institute, Russia)

10:15 – 10:45 Coffee break

10:45 Session NVMs II. Chair: Andrea Cester, Università di Padova, Italy

10:45 - Electrical Characterization of Metal-Oxide-High-k Dielectric-Oxide-Semiconductor (MOHOS) Structures for Memory Applications, H. Hsu and J. Ya-min Lee, (Tsing-Hua University, Hsinchu, Taiwan, Republic of China)

11:00 - Experimental study of electron transport in multilayered structures, G. Tao, C. Ouvrard, H. Chauveau and S. Nath, (Philips Semiconductors, Nijmegen, The Netherlands)

11:15 - Reliability of HTO based high voltage gate stacks for Flash memories, Y. Raskin, A. Salameh, D. Betel and Y. Roizin, (Tower Semiconductor Ltd., Migdal HaEmek, Israel)

11:30 - Structural and electrical properties of annealed Al₂O₃ thin films as inter-poly dielectric for Flash Memory applications, C. Wiemer¹, S. Spiga¹, E. Bonera¹, M. Fanciulli¹, R. Piagge², M. Alessandri², M. Caniatti², G. Pavia², E. Cadelano³, G. M. Lopez³, V. Fiorentini³, (¹CNR-INFN, Agrate Brianza, Italy; ²STMicroelectronics, Agrate Brianza, Italy; ³CNR-INFN, Cagliari University, Italy)

11:45 - The characterization of retention properties of metal-ferroelectric (PbZr_{0.53}Ti_{0.47}O₃)-insulator (Dy₂O₃, Y₂O₃)-semiconductor devices, Yu-Di Su and J. Ya-min Lee, (Tsing-Hua University, Hsinchu, Taiwan, Republic of China)

12:00 - Comparison of Deposition Models for a TEOS CVD Process, S. Holzer¹, A. Sheikholeslami², M. Karner², and T. Grasser¹, (¹Christian Doppler Laboratory for TCAD in Microelectronics at the Institute for Microelectronics; ²Institute for Microelectronics, Wien, Austria)

12:15 - Charge accumulation in the dielectric of the nanocluster NVM MOS structures under anti- and unipolar W/E window formation, V. Turchanikov^a, A. Nazarov^a, V. Lysenko^a, V. Ostahov^a, O. Winkler^b, B. Spangenberg^b, H. Kurz^b, (^aLashkaryov Institute of Semicond. Physics, NAS of Ukraine, Ukraine; ^bInstitute of Semiconductor Electronics, RWTH Aachen University, Aachen, Germany)

12:30 CLOSING ADDRESS

POSTER SESSION

Monday June 26, 17:30-20:00

- P1 **Influence of the SiO₂ layer thickness on the degradation of HfO₂/SiO₂ stacks subjected to static and dynamic stress conditions**, E. Amat*, R. Rodríguez, M. Nafria, X. Aymerich, J.H. Stathis^a Dept. d'Enginyeria Electrònica. Edifici Q. Universitat Autònoma de Barcelona, Bellaterra, Spain, ^aIBM Semiconductor Research and Development Center (SRDC), Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA.
- P2 **Effect of Oxide Breakdown on RS Latches**, R. Fernández^a, R. Rodríguez, M. Nafria, X. Aymerich
Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Bellaterra, Barcelona, Spain, ^aalso with Departament d'Educació Generalitat de Catalunya, IES Castellarnau, Sabadell.
- P3 **Low dielectric constant mesoporous silica thin films**, R.A. Farrell^{1,2}, J.D. Holmes^{1,2,3}, K. Cherkaoui², P.K. Hurley², M.A. Morris^{1,2,3} ¹Materials and Supercritical Section, Dept. of Chemistry, University College Cork, Ireland, ²Tyndall National Institute, Lee Maltings, University College Cork, Ireland, ³Centre for Research on Adaptive Nanostructures and Nanodevices (CRANN), Trinity College, Dublin, Ireland.
- P4 **Development of a permittivity extraction method for ultra low k dielectrics integrated in advanced interconnects**, O. Cueto, M. Assous, F. de Crécy, A. Toffoli, D. Bouchu, M.Fayolle, F. Boulanger, CEA-LETI, Grenoble, France.
- P5 **Current oscillations in Si nanocrystals embedded in SiO₂ observed by Tunneling Atomic Force Microscopy**, J. Carreras^{3,1}, L. Ricciardi¹, P. Fiorenza¹, R. Puglisi¹, G. Bimbo², V. Ancarani², M. Porti⁴, M. Nafria⁴, C. Gerardi², B. Garrido³, S. Lombardo¹ ¹CNR-IMM, Catania, Italy; ²STMicroelectronics, Catania, Italy; ³EME, Departament d'Electrònica, Universitat de Barcelona, Barcelona, Spain; ⁴Universitat Autònoma de Barcelona, Spain.
- P6 **Parameters extraction of hafnium based gate oxide capacitors**, T. Nguyen¹, C. Busseret¹, L. Militaru¹, D. Aimé^{1,2}, N. Baboux¹, C. Plossu¹ ¹LPM, UMR CNRS, INSA de Lyon, Villeurbanne, France, ²STMicroelectronics, Crolles, France.
- P7 **Charge Trapping Characterization of the HfO₂ / p-Si Interfaces at Cryogenic Temperatures**, I.P. Tyagulskyy, I.N. Osiyuk, V.S.Lysenko, A.N. Nazarov, * S. Hall, O. Buiu, Y. Lu, ** R. Potter, P. Chalker *** V.E. Lashkaryov Institute of Semiconductor Physics, National Academy of Sciences of Ukraine, Kiev, Ukraine; **Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, United Kingdom; ***Department of Engineering, University of Liverpool, Liverpool, United Kingdom.
- P8 **Optical and electrical characterization of hafnium oxide deposited by Liquid Injection Atomic Layer Deposition (LI-ALD)**, P. Taechakumput^a, S. Taylor^a, O. Buiu^a, D. L. Ram^b, R. J. Potter^b, P. R. Chalker^b, A. C. Jones^b ^aDepartment of Electrical Engineering and Electronics, University of Liverpool, UK, ^bDepartment of Material Science and Engineering, University of Liverpool, UK, ^cDepartment of Chemistry, University of Liverpool, UK.
- P9 **X-ray photoelectron spectroscopy study of ion assisted growth of ultrathin HfO₂/Si Dielectric films**, S.McDonnell¹, G.Hughes¹, K.Cherkaoui², P.K.Hurley², R.Dunne³, S.Cosgrave³, M. Tiernan³ ¹School of Physics Sciences, Dublin City University, Glasnevin, Dublin, Ireland, ²Tyndall National Institute, Lee Maltings, Cork, Ireland, ³Intel Ireland, Leixlip, Co Kildare, Ireland.
- P10 **Interface states and traps in thin N₂O-grown oxynitride/oxide di-layer for PowerMOSFET devices**, G. Currò¹, M. Camalleri¹, D. Cali¹, F. Manforte², F. Neri² ¹STMicroelectronics, Catania, Italy, ²Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate, Università di Messina, Messina, Italy.
- P11 **LOCOS induced stress effects on SOI bipolar devices**, S. Privitera, R. Modica, V. Cerantonio, G. Fallica, R&D department, Micro, Power, Analog (MPA) Group, STMicroelectronics, Catania, Italy.
- P12 **Measurement of the hot carrier damage profile in LDMOS devices stressed at high drain voltage**, D. Corso¹, S. Aurite¹, E. Sciacca¹, D. Naso¹, S. Lombardo¹, A. Santangelo², M. C. Nicotra², S. Cascino² ¹CNR-IMM, Catania, Italy; ²STMicroelectronics, Catania, Italy.

- P13 **Carrier trapping in thin N₂O-grown oxynitride/oxide di-layer for PowerMOSFET devices**, G. Currò¹, M. Camalleri¹, D. Cali¹, F. Manforte², F. Neri² ¹STMicroelectronics, Catania, Italy; ²Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate, Università di Messina, Messina, Italy.
- P14 **Tuneable electrical properties of hafnium aluminate gate dielectrics deposited by metal organic chemical vapour deposition**, Y. Lu¹, O. Bui¹, I. Mitrovic¹, S. Hall¹, R. J. Potter², P. Chalker² ¹Department of Electrical Engineering and Electronics, University of Liverpool, Liverpool, UK, ²Department of Engineering (Material Science Division), University of Liverpool, Liverpool, UK.
- P15 **Ferroelectric Characteristic of Group IV Elements added SrBi₂Ta₂O₇ Thin Films**, S. Tamura, Y. Omura, High-Technology Research Center and Faculty of Engineering, Kansai University, Osaka, Japan.
- P16 **Influence of Argon Ion Assist on the Electrical Properties of Ultra-Thin HfO₂ on Si(100) Formed by Electron Beam Deposition**, K. Cherkaoui^a, P.K. Hurley^a, A. Negara^a, S. McDonnell^b, G. Hughes^b, R. Dunne^c, S. Cosgrave^c, M. Tiernan^c ^aTyndall National Institute, Lee Maltings, Cork, Ireland, ^bSchool of Physics Sciences, Dublin City University, Glasnevin, Dublin, Ireland, ^cIntel Ireland, Leixlip, Co Kildare, Ireland.
- P17 **An Investigation on Capture Cross-Section of Surface State of Metal-Oxide-Semiconductor Field-Effect Transistors Using HfO₂ Gate Dielectrics**, F. C. Chiu¹, W. C. Shih², J. Y. Lee², H. L. Hwang² ¹Department of Electronics Engineering, Ming Chuan University, Taoyuan, Taiwan, Republic of China, ²Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, Taiwan, Republic of China.
- P18 **Development of SrTiO₃ (STO)-Y₂O₃ bilayer dielectrics for MIM capacitor elaboration with improved electrical properties**, M. Kahn, C. Vallee, E. Defay, M. Bonvalot, C. Dubourdieu, J.R. Plaussy, T. Baron, LTM/CNRS, Grenoble, France.
- P19 **Total Irradiated Dose reliability of thin SiO₂ in PowerMOSFET devices**, G. Currò[†], A. Cascio[†], A. Cavagnoli^{*} [†]STMicroelectronics, Catania, Italy, ^{*}TopRel srl, Rome, Italy.
- P20 **Double-Logarithm 1/E Model: A New Empirical Unified Oxide Reliability Model**, L. M. Wang, Jiangsu College of Information Technology, Jiangsu, China.
- P21 **Evaluation of the generation mechanisms at surface and in the bulk of the silicon by current transient technique**, G. Barletta, G. Currò, ST Microelectronics, Catania, Italy.
- P22 **Charge Loss Acceleration In Single-Poly OTP-NVM under illumination**, L. Montagner-Morancho[§], D. Ramis, G. Sarabayrouse, J.L. Chaptal[#] LAAS-CNRS, Toulouse, France, [#]Freescale Semiconducteurs France SAS, Toulouse, France, [§] presently at ATMEL-ZI Rousset, Rousset, France.
- P23 **Correlation between infrared transmission spectra and the interface trap density of SiO₂ films**, V. Em. Vamvakas^{1*}, M. Theodoropoulou², S. N. Georga², C. A. Krontiras², M. N. Pisanias² ¹Institute of Microelectronics, NCSR "Demokritos", Athens, Greece, ²University of Patras, Dept. of Physics, Patras, Greece.
- P24 **Optimization and performance of Al₂O₃/GaN metal-oxide-semiconductor structures**, K. Čičo¹, J. Kuzmík^{1,2}, D. Gregušová¹, T. Lalinský¹, D. Pogany², K. Fröhlich¹ ¹Institute of Electrical Engineering SAS, Bratislava, Slovakia, ²Institute for Solid State Electronics TU Vienna, Vienna, Austria.
- P25 **Nitrogen bonding configurations near the oxynitride/silicon interface after oxynitridation in N₂O ambient of a thin SiO₂ gate**, F. Monforte^{*}, M. Camalleri[†], D. Cali[†], G. Currò[†], E. Fazio^{*}, F. Neri^{*} ^{*}Dipartimento di Fisica della Materia e Tecnologie Fisiche Avanzate, Università di Messina, Messina, Italy, [†]STMicroelectronics, Catania, Italy.
- P26 **Peculiarities of electron tunnel injection to the drain of EEPROMs**, N. Baboux¹, C. Busseret¹, C. Plossu¹, P. Boivin² ¹Laboratoire de Physique de la Matière, UMR CNRS, Villeurbanne, France, ²STMicroelectronics, Rousset, France.
- P27 **Electronic and dielectric properties of CaCu₃Ti₄O₁₂ revisited**, P. Alippi^{*}, V. Fiorentini^{**}, A. Filippetti^{**} ^{*}CNR-IMM, Catania, Italy, ^{**}CNR/INFN – SLACS and University of Cagliari, Cagliari, Italy.
- P28 **Gate oxide engineering with high-κ dielectrics viewed with nanoanalytical transmission electron microscopy**, S. Schamm¹, C. Bonafos¹, G. Scarel², M. Fanciulli², P.E. Coulon¹ ¹CEMES-CNRS, Toulouse, France, ²MDM-INFN-CNR National Laboratory, Agrate Brianza (MI), Italy, ³Institute of Microelectronics, NCSR 'Demokritos', Greece.

- P29 **Structural and Electrical Properties of Bismuth Pyrochlore Bi_3NbO_7 Thin Films by Low Temperature Metalorganic Chemical Vapor Deposition**, S.Y. Jeon, N. J. Seong, S. G. Yoon, Department of Materials Science and Engineering, Chungnam National University, Daeduk Science Town, Daejeon, Korea.
- P30 **Volatility and Vapourisation Characterisation Of New Precursors**, S. Rushworth, H. Davies, A. Kingsley, R. Odedra, Epichem Limited, Bromborough, Wirral, UK.